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REMARKS

Claims 1-4, as amended, remain herein.

Applicants appreciate the statements in the Office Action that claims 2 and 4 are allowable.

Minor, editorial changes have been made in claims 1 and 3.

1. Objections were stated to claim 2. Each informality has been amended, thereby mooting those objections. Antecedent basis in claim 2 is now clear.

2. Claims 1 and 3 were rejected under 35 U.S.C. §103(a) over Chow et al. U.S. Patent 5,617,486 and Vassiliadis et al. U.S. Patent 4,924,422.

The Office Action cites Chow '486 as allegedly disclosing a vector processing system including a decision step for computing whether an arithmetic operation is to be performed when target data is obtained, including an arithmetic control to execute vector arithmetic and output a result, but admits that Chow '486 does not disclose the computing and decision steps performed in parallel, and found it necessary to cite Vassiliadis '422 as

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allegedly teaching same. Chow '486 discloses a pattern recognition system including a method for pattern recognizing data input on a continuing basis, using Markov Models. Vassiliadis '422 discloses a method for determining that a comparison result of two values is zero (equivalent) without the use of an adder.

The Office Action alleges that it becomes possible to perform "calculation and decision" in parallel if the method of vector arithmetic disclosed in Chow '486 is modified by using the method taught by Vassiliadis '422.

However, the presently claimed invention comprises an arithmetic decision step of computing and deciding whether an arithmetic process is to be executed in parallel with obtaining an arithmetic processing target data, and an arithmetic control step of exerting arithmetic control to execute the arithmetic process for the arithmetic processing target data and output a result of the arithmetic process or output the target data without executing the arithmetic, according to a result decided in the arithmetic decision step as recited in claims 1 and 3. Thus, the invention enables performing vector arithmetic

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processing in a conditional arithmetic process. Therefore, conditional arithmetic can be divided into a process of (1) deciding whether the arithmetic should be performed or not and (2) controlling whether the arithmetic is to be executed or not according to the decided result, followed by outputting (3) a result of the arithmetic process or (4) the originally inputted data itself without executing the arithmetic process. Because the flow of a pipeline is not interrupted by performing these processes in parallel, high speed vector arithmetic can be carried out. The phrase "operation in parallel" here indicates a status that N+1-th data is being processed in an arithmetic decision step while N-th data is being processed in an arithmetic control step.

Therefore, contrary to the suggestion in the Office Action, the presently claimed invention cannot be obtained merely from the fact that calculation and decision can be performed in parallel.

For the foregoing reasons, neither Chow '486 nor Vassiliadis '422 contains any teaching, suggestion, reason, motivation or incentive that would have led one of ordinary

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skill in the art to applicants' claimed invention. Nor is there any disclosure or teaching in either of these references that would have suggested the desirability of combining any portions thereof effectively to anticipate or suggest applicants' presently claimed invention. Accordingly, reconsideration and withdrawal of this rejection are respectfully requested.

All claims 1-4 are now proper in form and patentably distinguished over all grounds of rejection stated in the Office Action. Accordingly, allowance of all claims 1-4 is respectfully requested.

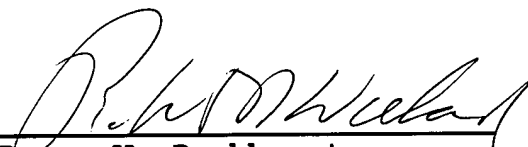
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Should the Examiner deem that any further action by the applicants would be desirable to place this application in even better condition for issue, the Examiner is requested to telephone applicants' undersigned representatives.

Respectfully submitted,

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